IFW
AF

PATENT
Attorney Docket No.: ALSC-00300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Group Art Unit: 2814
Ritu Shrivastava	Examiner: Nathan W. Ha
Serial No.: 09/315,599	**TRANSMITTAL LETTER**
Filed: May 20, 1999	
For: **A METHOD OF AND APPARATUS FOR INTEGRATING FLASH EPROM AND SRAM CELLS ON A COMMON SUBSTRATE**	162 North Wolfe Road Sunnyvale, California 94086 (408) 530-9700
	Customer Number 28960

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed please find an Appeal Brief in triplicate for filing with the U.S. Patent and Trademark Office. Also attached is a check in the amount of $500.00 to cover the appeal brief filing fee.

The Commissioner is authorized to charge any additional fee or credit any overpayment to our Deposit Account No. 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: December 20, 2004

By: Jonathan O. Owens
Jonathan O. Owens
Reg. No.: 37,902

Attorneys for Applicant

CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP.

Date: 12-20-04 By: Jonathan D. Rosen

PATENT
Attorney Docket No.: ALSC-00300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Group Art Unit: 2814
Shrivastava	Examiner: Nathan W. Ha
Serial No.: 09/315,599	**APPEAL BRIEF**
Filed: May 20, 1999	162 North Wolfe Road Sunnyvale, California 94086 (408) 530-9700
For: **METHOD AND APPARATUS FOR INTEGRATING FLASH EEPROM AND SRAM CELLS ON A COMMON SUBSTRATE**	Customer No.: 28960

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In furtherance of the Applicant's Notice of Appeal filed on October 20, 2004, this Appeal Brief is submitted herewith in triplicate. This Appeal Brief is submitted in support of the Applicant's Notice of Appeal, and further pursuant to the final rejection mailed on July 20, 2004, in which claims 1, 4-6, 9, 10, and 21-28 were rejected. The Applicant submits this Appeal Brief to the Board of Patent Appeals and Interferences in compliance with the requirements of 37 C.F.R. § 41.37, as stated in *Rules of Practice Before the Board of Patent Appeals and Interferences (Final Rule)*, 69 Fed. Reg. 49959 (August 12, 2004). The Applicant contends that the rejections of Claims 1, 4-6, 9, 10, and 21-28 in this proceeding are in error and are overcome by this appeal.

12/28/2004 ZJUHAR1 00000042 09315599
01 FC:1402 500.00 OP

CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP

Date: 12-20-04 By: Juan D. Rascon

I. REAL PARTY IN INTEREST

As the assignee of the entire right, title, and interest in the above-captioned patent application, the real party in interest in this appeal, is:

Alliance Semiconductor
3099 North First Street
San Jose, California 95134

The assignment is made by assignment documents recorded on May 20, 1999, on reel/frame number 00990/0362.

II. RELATED APPEALS AND INTERFERENCES

The Applicant is not aware of any other appeals or interferences related to the present application.

III. STATUS OF THE CLAIMS

Claims 1, 4-6, 9, 10, 18, and 21-28 are pending in this case and stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,605,853 to Yoo et al. (hereinafter, Yoo, a copy of which is attached as Exhibit A) in view of U.S. Patent No. 5,679,599 to Mehta (hereinafter, Mehta, a copy of which is attached as Exhibit B). Claims 2, 3, 5-8, and 11-17 have been canceled. Within this Appeal Brief, claims 1, 4-6, 9, 10, 18, and 21-28 are appealed.

IV. STATUS OF THE AMENDMENTS FILED AFTER FINAL REJECTION

No amendments have been filed after the Advisory Action mailed on October 6, 2004.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention disclosed in the present application S/N 09/315,599 (the '599 application) is directed to a device comprising an SRAM device and an EPROM device on a common substrate, with each device isolated from the other by an isolation structure tailored to the specific device. Some of the advantages of this device are described in the Specification at, for example, page 5, line 19, to page 6, line 13, and include (1) reduced size of the entire semiconductor package containing both the SRAM device and the EPROM device, (2) increased durability and reliability of the semiconductor package, and (3) increased communication speed and accuracy between the SRAM device and the EPROM device.

The elements of claim 1, directed to one embodiment of the present invention, are described in the Specification at page 9, lines 17-24, and the accompanying Figure 14. The device shown there comprises a common substrate 100, an SRAM device (outlined by the dashed lines over the area labeled 230) implemented on the common substrate 100 and isolated by a shallow trench 220 filled with an insulating oxide substance 225 (thus forming a shallow trench isolation structure), and a flash EPROM device (outlined by the dashed lined over the area labeled 210) implemented on the common substrate 100 and isolated by a field oxide layer 200 (thus forming a local oxidation of silicon or LOCOS isolation structure).

All of the following independent claims–5, 9, 18, 23, and 26–are also described by reference to Figure 14. The explanations of the SRAM device and flash EPROM device are identical to those offered for claim 1 and are not repeated below.

Claim 5 is directed to another embodiment of the present invention. Claim 5 is directed to a system containing different types of isolation structures. The system comprises a common substrate 100, an SRAM device, and a flash EPROM device. The common substrate 100 has a first portion 102 including an STI isolation structure 225 and a second portion 104 including a LOCOS isolation structure 200. The STI isolation structure 225 and the LOCOS isolation structure 200 are implemented non-concurrently. The SRAM device is formed on the first portion 102 of the substrate 100; and the flash EPROM device is formed on the second portion 104 of the substrate 100.

Claim 9 is directed to another embodiment of the present invention. Claim 9 is directed to a semiconductor device comprising a common substrate 100, an SRAM device, and a flash EPROM device. The common substrate 100 has a first portion 102 including an STI isolation structure 220 and a second portion 104 including a LOCOS isolation structure 200. The STI isolation structure and the LOCOS isolation structure are implemented non-concurrently. The

SRAM device is implemented on the first portion 102 of the substrate 100; and the flash EPROM device is implemented on the second portion 104 of the substrate 100.

Claim 18 is directed to another embodiment of the present invention. The device defined in claim 18 comprises a common substrate 100 which underlies both a first portion 102 and a second portion 104. The first portion 102 comprises an SRAM device over a first single device layer that comprises a first active region 230 and an STI isolation structure 220. The second portion 104 comprises a flash EPROM device over a second single device layer that comprises a second active region 210 and a LOCOS isolation structure 200. As described in more detail below, the use of a single device layer for each portion provides a structure that has advantages in both isolation and manufacturing.

One basis for this Appeal is that in the final Office Action, the rejections did not even address the elements of claim 18 that recite single device layers. Within the rejections there is no mention of these elements at all and thus, the burden to prove that claim 18 is unpatentable has not been met.

Claim 23 is directed to another embodiment of the present invention. The semiconductor device defined in claim 23 comprises a common substrate 100 having a first area 102 and a second area 104. The first area 102 includes an STI isolation structure 225; the second area 104 includes a LOCOS isolation structure 200. The second area 104 has an outer portion, containing the labels 200 and flanking the block labeled "FLASH." The outer portion extends a first depth into the common substrate 100. As described in the Specification, 200 refers to the entire field oxide layer. The second area 104 also has an inner portion that includes the active region 210 and that extends a first depth into the common substrate 100. The first depth is larger than the second depth. That is, the depth of the LOCOS portion, below the labels 200, for example, extends deeper into the common substrate 100 than does the portion under the section labeled 210. An SRAM device is positioned on the first area 102 of the common substrate 100 (above the area labeled 230) and a flash EPROM device is positioned on the second area 104 of the common substrate 100 (above the area labeled 210), all as shown in Figure 14.

Claim 26 is directed to another embodiment of the present invention. The system defined in claim 26 contains a semiconductor device having a plurality of isolated structures. The system comprises a common substrate 100, an SRAM device (described above), and a flash EPROM device (also described above). The common substrate 100 has a first area 102 including an STI isolation structure 225 and a second area 104 including a LOCOS isolation structure 200. The second area 104 has an outer portion extending a first depth into the substrate 100 and an inner

portion including an active region 210 extending a second depth into the substrate 100. The first depth is larger than the second depth. The SRAM device implemented on the first area 102 of the substrate 100. The flash EPROM device implemented on the second area 104 of the substrate 100.

In the final Office Action, the structure recited in claims 23 and 26 is addressed, but the first depth is confused with the second depth. Thus, a determination that the structure recited in claims 23 and 26 was found in the prior art is incorrectly reached. The Applicant pointed out this error in its Amendment and Response to Final Office Action mailed on July 20, 2004. The arguments made in that Amendment and Response were ignored.

VI. GROUNDS OF REJECTION AND OTHER MATTERS TO BE REVIEWED ON APPEAL

The following issues are presented in this Appeal Brief for review by the Board of Patent Appeals and Interferences:

1. Whether claims 1, 4-6, 9, 10, 18 and 21-28 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoo in view of Mehta.
2. Whether independent claim 18 (and thus its dependent claims 21 and 22) is allowable because the claim limitations that the Applicant repeatedly argued distinguish claim 18 over the prior art were not addressed within the Office Action.
3. Whether independent claims 23 and 26 (and thus their corresponding dependent claims 24-25 and 27-28) are allowable because the structure of claim limitations was misread and thus the claims were improperly rejected based on that misreading.

VII. ARGUMENT

In section A of the discussion that follows, the Applicant will explain why claims 1, 4-6, 9, 10, 18, and 21-28 are allowable over the cited references. Within the explanations of section A, the Applicant will also point out those arguments that were either ignored or misconstrued during examination. For example, the Office Actions did not address the Applicant's arguments that claim 18 recites structure not found in the prior art. Furthermore, within the Office Actions, the claim limitations recited in claims 23 and 26 were misconstrued. In section B, the Applicant cites case law supporting its argument that, because the Office Action did not address claim limitations recited in claim 18 but not found in the prior art, claim 18, and this its dependent claims 21 and 22, are allowable.

In the discussions that follow, the Applicants have bolded the title of Responses and appropriate pages numbers in which it offered arguments that were not addressed by the PTO during prosecution of this case. These arguments were offered (1) in a response filed May 19, 2004, and titled *Amendment and Response to Office Action Mailed on February 19, 2004*, (the May 2004 Response), and again (2) in a response filed September 20, 2004, and titled *Amendment and Response to Final Office Action Mailed on July 20, 2004* (the July 2004 Response). To make the following text easier to read, only the May 2004 Response is cited.

A. REJECTIONS UNDER 35 U.S.C. § 103(a)

Grounds for Rejection

Within the Office Action, claims 1, 4-6, 9, 10, 18, and 21-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 5,605,853 to Yoo *et al.* ("Yoo") in view of U.S. Patent Number 5,679,559 to Mehta ("Mehta").

Outline of Arguments

In the discussion that follows, the Applicant first discusses Yoo, Mehta, and their proposed combination. The Applicant then analyzes the pending claims and their limitations and explains why Yoo, Mehta, and their combination do not disclose, suggest, or provide any motivation for these limitations.

1. Yoo does not teach a structure having (1) a single device layer as taught in the present invention, or (2) an isolation structure with relative depths as taught in the present invention, or (3) both a LOCOS isolation structure and an STI isolation structure.

Yoo is directed to "[a]n integrated process for forming a 4T SRAM and a floating gate memory, with logic, on the same integrated circuit." (Yoo, Abstract) In Figure 7, Yoo discloses an SRAM region 50 formed over a substrate 10 and isolated by a field oxide region 12. The field oxide region 12 is formed below a gate electrode 16 and contacts 28. An active region 22 is formed in a second device layer, the substrate 10. **As stated at page 5 of the May 2004 Response**:

> The SRAM region 50 is thus not formed over a single device layer that comprises a first active region and an STI isolation structure. The isolation structure 12 has an inner portion at a first depth and an outer portion at a second depth, less than the first depth. The isolation structure thus narrows at its edges, having what is called a bird's beak shape.

In accordance with the method, Yoo teaches forming an SRAM, a floating gate memory, and a logic device on the same integrated circuit. Specifically, Yoo teaches a method of forming simultaneously an SRAM and an EEPROM on the same integrated circuit, using a LOCOS isolation process. (Yoo, col. 3, lines 51-55). Yoo teaches a method of forming a plurality of field isolation regions using a LOCOS isolation process. (Yoo, col. 3, line 55-60) The structure disclosed in Figure 7 of Yoo comprises an SRAM 50 and a gate memory 70 separated by field oxidation regions 12.

Yoo does not teach or suggest that an SRAM and an EEPROM can be formed on the same IC, using a shallow trench isolation (STI) process. Neither does Yoo teach or suggest that an SRAM and an EEPROM can be formed on the same IC, using a combination of a LOCOS and an STI isolation process. As indicated by Yoo, in column 2, lines 18-26, a combination of an SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* (Yoo, column 2, lines 23-26) In column 2, lines 18-26, Yoo states:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining an SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating an SRAM and an EEPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Further, Yoo teaches away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate.

2. Mehta does not teach a structure having (1) a single device layer as taught in the present invention, or (2) an isolation structure with relative depths as taught in the present invention, or (3) both a LOCOS isolation structure and an STI isolation structure.

Mehta teaches a device and method for isolating regions of a circuit device in a semiconductor substrate. The method comprises the following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. (Mehta, Abstract and col. 4, line 46 to col. 6, line 49)

In Figure 18, Mehta discloses a structure formed in accordance with the method. Figure 18 discloses a substrate 100 containing a first trench 242 and a second trench 240, isolated from each other by a thin layer of oxide (unnumbered). **As stated at pages 6-7 of the May 2004 Response**:

> The portions used to isolate and form the active regions are thus formed from multiple device layers. The first trench 242 has a center portion at a first depth and an outer portion at a second depth, less than the first depth. The first depth thus has a classic bird's beak shape. The disadvantages of bird's beaks are well known in the art, and at column 6, lines 34-41, Mehta teaches an embodiment for minimizing the negative effects of a bird's beak: "Partial nitride encapsulation is shown in FIG. 18; total nitride encapsulation occurs if spacers 180 are not etched back. No nitride encapsulation occurs if the spacers are etched off completely. Nitride encapsulation tends to reduce the bird's beak effect which is commonly seen in LOCOS processes."
>
> Mehta further teaches at column 7, lines 8-13: "Significant encroachment or ΔW of the bird's beak region can reduce the effective area of the active region between the isolation areas. By incorporating nitride encapsulation in conjunction with the method and structure of the present invention, encroachment can be reduced." As described below, embodiments of the present invention provide a structure that advantageously do[es] not have a bird's beak and thus do[es] not need to rely on nitride encapsulation or other additional isolation techniques.

Mehta does not teach or suggest combining a LOCOS isolation structure and an STI isolation structure. Instead, Mehta teaches a LOCOS region and a field oxidized trench region (*see, e.g.*, Mehta, col. 6, lines 21-22), not an STI region. At column 7, lines 42-25, Mehta makes clear that it does not teach STI: "Finally, in shallow trench isolation, a critical planarization mask is generally needed to reduce such dishing. *In the present method and apparatus*, no such critical mask is needed" (italics added).

Still, at page 3 of the final Office Action, it is stated that "Furthermore, the trench isolation is needed in densely packed regions where the active spacing is small, such as a memory array in a DRAM, SRAM, or EEPROM; see [Mehta] also, col. 4, lines 50-56." This is simply not true. Densely packed regions often rely on other isolation structures. And while other isolation structures are used, none combine STI and LOCOS as taught in the present invention.

3. There is no motivation to combine Mehta and Yoo because Mehta teaches against STI.

The M.P.E.P. makes clear that "[i]t is improper to combine references [to support a § 103 rejection] where the references teach away from the combination." M.P.E.P. § 2145(X)(D)(2) (Rev. 2, May 2004) (citing *In re Grasselli*, 713 F.2d 731, 743 (Fed. Cir. 1983)). The case against a § 103 rejection is even stronger here, where neither Yoo nor Mehta even teaches an STI

structure. Indeed, Mehta teaches against using STI structures in general. For example, at column 2, lines 50-58, Mehta states:

> However, shallow trench isolation (STI) is relatively complex because an anisotropic etch must be used to define the trench, the trench must be etched deeply into the silicon, and filling the trench with the isolation material can raise additional processing issues in preparing the integrated circuit. STI also results in relatively sharp corners at the edges of the trench at the silicon surface. This can result in electrical field leakage at these corners and gate oxide quality problems.

In the Summary of the Invention, Mehta states that one "object of the invention is to provide a process which provides significant advantages over shallow trench isolation and combination of shallow trench isolation and local oxidation processes." (Mehta, col. 3, lines 56-59) Later, Mehta states that "[STI] technology . . is replete with problems." (*Id.*, col. 7, lines 21-22)

Mehta distinguishes its invention over STI, and thus teaches away from STI, by stating that its invention "preserves the familiar and well-characterized interface between active regions and isolation regions in the LOCOS field. No edge oxide quality problems would therefore result." (*Id.*, lines 26-29) Mehta further states that "[STI] is subject to trench corner leakage" (*id.*, line 30-31) and produces "dishing [which causes] thinning of the isolation in wide-trench regions" (*id.*, lines 38-39). Thus, Mehta teaches away from structures that use STI structures alone or in combination with any other isolation structures.

4. The final Office Action improperly finds motivation to combine Mehta and Yoo.

Within the final Office Action, it is concluded that it would have been obvious to use the STI isolation technique as taught by Mehta in the substrate of Yoo. Specifically, it is stated within the final Office Action, "[I]t would have been obvious to one of ordinary skill in the art at the time of the invention was made to use STI isolation technique as taught by Mehta in Yoo et al. substrate in order to scale the minimum spacing between regions." The Applicant respectfully disagrees with this conclusion.

As discussed above, Mehta teaches away from the use of STI. Further, to support this conclusion, a *prima facie* case of obviousness must be demonstrated. No such demonstration has been made here. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation demonstrated, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine

the teachings of the references. Second, there must be a demonstration that the combination of the prior art references would result in a reasonable expectation of success. Third, the combination of the prior art references must teach or suggest all the claim limitations. (M.P.E.P § 2142 - 43.)

First, there is no suggestion or motivation to combine Yoo and Mehta. Yoo teaches away from including an SRAM and an EEPROM on the same IC, isolated by a combination of a LOCOS and a second isolation technique. Furthermore, Mehta does not teach or otherwise indicate that the first and second isolation techniques can be applied to isolate an SRAM and an EEPROM on a common IC. Therefore, it would not have been obvious to one skilled in the art to combine the teachings of Yoo and Mehta. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Within the Office Action, there has not been any reference to any teaching, hint or suggestion in either Yoo or Mehta suggesting the desirability of combining these two references.

Further, there is no indication in the prior art that a combination of Yoo and Mehta would result in a reasonable expectation of success. As indicated by Yoo, in column 2, lines 18-26, a combination of an SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* (Yoo, column 2, lines 23-26) Furthermore, the teachings of Mehta do not indicate or suggest that the first and second isolation techniques can be applied to isolate an SRAM and an EPROM on a common IC. The combination of the teachings of Yoo and Mehta would not have resulted in a reasonable expectation of success. Therefore, the combination of the teachings of Yoo and Mehta does not render the current invention obvious.

Even if considered proper, the combination of Yoo and Mehta does not teach the claimed invention. In contrast to the teachings of Mehta, Yoo and their combination, the present invention teaches a system for *independently* or *non-concurrently* integrating SRAM cells and flash EPROM cells onto a single silicon substrate. As discussed above, neither Mehta, nor Yoo, nor their combination teaches or suggests forming an SRAM and an EPROM on a single substrate using a combination of a LOCOS isolation process and an STI isolation process. In column 2, lines 18-26, Yoo states the following:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining an SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating an SRAM and an EPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Therefore, it would not have been obvious to one skilled in the art, that Yoo could have been combined with Mehta to disclose the current invention. Further, Yoo appears to be teaching away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate. Therefore it would not have been obvious to one skilled in the art from the teachings of Yoo, that a LOCOS and STI isolation process could have been used to form an SRAM and an EEPROM on a common substrate. Further, as discussed above, Mehta teaches away from the use of the STI isolation technique. Accordingly, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a Flash EPROM device isolated by a LOCOS isolation structure.

5. The present invention comprises a structure different from that disclosed in both Mehta and Yoo.

The present invention is directed to semiconductor devices and systems comprising an SRAM device and an EPROM device on a single substrate. The SRAM device is formed on an STI isolation structure and the EPROM device is formed on a LOCOS isolation structure. The present invention thus provides on a single substrate both low-voltage devices and high-voltage devices. Such a structure has the advantages of smaller package size, less interference, and quicker transmission of data between the SRAM and EPROM cells. (Specification, page 10, line 24, to page 11, line 4)

6. The claims distinguish over the prior art.

The claims are grouped separately below to indicate that they do not stand or fall together.

a. Claims 1 and 4

The independent claim 1 is directed to a semiconductor device. The semiconductor device of claim 1 comprises a common substrate, an SRAM device implemented on the common substrate and isolated by an STI isolation structure, and a flash EPROM device implemented on the common substrate and isolated by a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently. As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. Within the Office Action it is stated that "Mehta discloses the first [isolation] technique is the STI technique and the second isolation technique is LOCOS isolation, as discussed in claim 1." The Applicant respectfully disagrees with this statement. Instead, Mehta teaches a LOCOS region and a field oxidized trench region. As discussed above, Mehta teaches away from using an STI isolation structure. For at least these reasons, claim 1 is allowable over the teachings of Yoo, Mehta and their combination.

Within the final Office Action, the limitation in claim 1 reciting "wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently" is characterized as a process limitation. Within the final Office Action, it is then stated that this language would carry no patentable weight.

While not agreeing with this characterization of the claim language as a process limitation, the Applicants contend that even if it were true, claim 1 recites additional structure that distinguishes it over the prior art. Thus, even accepting the characterization as accurate, claim 1 is still allowable over the cited references.

Claim 4 is dependent on the independent claim 1. As discussed above, claim 1 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 4 is also allowable as being dependent on an allowable base claim.

b. Claims 5 and 6

The independent claim 5 is directed to a system containing different types of isolation structures. The system of claim 5 comprises a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently, an SRAM device on the first portion of the substrate, and a flash EPROM device on the second portion of the substrate. As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. For at least these reasons, claim 5 is allowable over the teachings of Yoo, Mehta and their combination.

Within the final Office Action, the limitation in claim 5 reciting "wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently" is characterized as a process limitation. Within the final Office Action, it is then stated that this language would carry no patentable weight.

While not agreeing with this characterization of the claim language as a process limitation, the Applicants contend that even if it were true, claim 5 recites additional structure that distinguishes it over the prior art. Thus, even accepting the characterization as accurate, claim 5 is still allowable over the cited references.

Claim 6 is dependent on the independent claim 5. As discussed above, claim 5 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 6 is also allowable as being dependent on an allowable case claim.

c. Claims 9 and 10

The independent claim 9 is directed to a semiconductor device. The semiconductor device of claim 9 comprises a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently, an SRAM device implemented on the first portion of the substrate, and a flash EPROM device implemented on the second portion of the substrate. As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having a first portion with an STI isolation

structure and a second portion with a LOCOS isolation structure. For at least these reasons, claim 9 is allowable over the teachings of Yoo, Mehta and their combination.

Within the final Office Action, the limitation in claim 9 reciting "wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently" is characterized as a process limitation. Within the final Office Action, it is then stated that this language would carry no patentable weight.

While not agreeing with this characterization of the claim language as a process limitation, the Applicants contend that even if it were true, claim 9 recites additional structure that distinguishes it over the prior art. Thus, even accepting the characterization as accurate, claim 5 is still allowable over the cited references.

Claim 10 is dependent on the independent claim 9. As discussed above, claim 9 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 10 is also allowable as being dependent on an allowable case claim.

d. Claims 18, 21, and 22

The independent claim 18 is directed to a semiconductor device. The semiconductor device of claim 18 comprises a common substrate, a first portion formed on the common substrate, and a second portion formed on the common substrate. The first portion comprises an SRAM device *over a first single device layer.* The first single device layer comprises a first active region and an STI isolation structure. The second portion comprises a flash EPROM device *over a second single device layer.* The second single device layer comprises a second active region and a LOCOS isolation structure.

As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests an SRAM device over *a single device layer* comprising a first active region and an STI isolation structure and a flash EPROM device *over a single device layer* comprising a second active region and a LOCOS isolation structure. For at least these reasons, claim 18 is allowable over Mehta, Yoo, and their combination.

The final Office Action confirms the Applicant's interpretation that the prior art shows the use of multiple device layers where the present invention uses only one. At page 3 of the final Office Action it is stated, "In regard to claims 24 and 27, Mehta or Yoo shows the first structure and second structure are contiguous, see Mehta's fig. 18." Thus, within the final Office

Action, one isolation structure comprises the thin layer of oxide, discussed above, a separate layer. Such a structure differs from that recited in claim 18.

i. The final Office Action does not challenge or even respond to the assertions in a previous Amendment and Response that the present invention distinguishes over the multiple device layer in the prior art.

At page 11 of the May 2004 Response, the Applicant argued that claim 18 was allowable because the prior art disclosed using multiple device layers. For example, at page 5 of the May 2004 Response, the Applicant argued that Yoo disclosed using multiple device layers to form an isolation structure and an active region, and at page 6 he argued that Mehta did the same. The final Office Action did not challenge let alone respond to these discussions.[1] As described below, M.P.E.P. § 707.07(f) and controlling case law require that independent claim 18 and its dependent claims 21 and 22 be allowed.

e. Claims 23-28

i. As to claims 23 and 26, the final Office Action confuses the difference between the first depth and second depth as recited in the claims.

The independent claim 23 is directed to a semiconductor device. The semiconductor device of claim 23 comprises a common substrate, an SRAM device implemented on the common substrate and formed over a first active region on a first isolated structure including an STI isolation structure, and a flash EPROM device implemented on the common substrate and formed over a second active region on a second isolated structure including a LOCOS isolation structure. It is further specified in claim 23 that the second isolated structure has an outer portion

[1] It is surprising that the PTO did not address the claim limitation and Applicant's arguments that distinguished claim 18 over the prior art. The PTO was well aware of this limitation. Indeed, in an advisory action mailed November 13, 2003, the PTO found that this added claim limitation raised new issues. In response, on December 10, 2003, the Applicant filed a Request for Continued Examination.

extending a first depth into the substrate and an inner portion including the second active region and extending a second depth into the substrate. It is also specified in claim 23 that the first depth is larger than the second depth.

As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests an isolated structure having an outer portion extending a first depth into a substrate and an inner portion including an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. Instead, Mehta discloses portions of two isolation structures each having an inner portion extending a first depth into a substrate and an outer portion extending a second depth into the substrate, where the second depth is larger than the first depth. Both structures result in a bird's beak. Within the Office Action it is stated that Mehta teaches "the first depth is larger than [the] second depth." Because both isolation structures in Mehta have a bird's beak shape, this characterization of Mehta is true only if the first depth is that of the outer portion. **This labeling of the depths is the opposite of that recited in claim 23.** When referring to the depth of the outer portion in Mehta as the first depth and the depth of the inner portion as the second depth, the same terminology used in claim 23, Mehta discloses a structure in which the first depth is smaller than the second depth. Mehta thus discloses a structure different from that recited in claim 23. Yoo also discloses a bird's beak structure which, for the same reasons given above, differs from the structure recited in claim 23. Accordingly, neither Yoo, nor Mehta, nor their combination teaches an isolated structure having an outer portion extending a first depth into a substrate and an inner portion including an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. For at least these reasons, claim 23 is allowable over Mehta, Yoo, and their combination.

Claims 24 and 25 both depend on claim 23. As described above, claim 23 is allowable over Mehta, Yoo, and their combination. Accordingly, claims 24 and 25 are also both allowable as depending on an allowable base claim.

Claim 26 is directed to a system containing a semiconductor device having a plurality of isolated structures. The system comprises a common substrate, an SRAM device, and a flash EPROM device. The common substrate has a first area including an STI isolation structure and a second area including a LOCOS isolation structure. The second area has an outer portion extending a first depth into the substrate and an inner portion including an active region and extending a second depth into the substrate. The first depth is larger than the second depth. The

SRAM device is implemented on the first area of the substrate; and the flash EPROM device implemented on the second area of the substrate.

Like claim 23, claim 26 recites an area including a LOCOS isolation structure that extends a first depth and a second depth in a manner that is not taught in the prior art. Accordingly, claim 26 is allowable over Yoo, Mehta, and their combination for the same reasons as claim 23.

Furthermore, because claims 27 and 28 depend on claim 26, they too are allowable as depending on an allowable base claim.

ii. The final Office Action does not challenge or even respond to the assertions in a previous Amendment and Response that the present invention distinguishes over the bird's beak structure in the prior art.

At pages 6-7 of the May 2004 Response the Applicant pointed out the existence of a bird's beak in the prior art and the discussion in the prior art about the disadvantages of the bird's beak. In the May 2004 Response the Applicant further explained that the claims in the present invention recite structure different from the prior art. The final Office Action did not challenge let alone respond to these discussions. As described in more detail below, M.P.E.P. § 707.07(f) requires that an examiner consider all arguments proposed by an applicant. Because claim limitations and supporting arguments were not considered in Office Actions here, M.P.E.P. § 707.07(f) and controlling case law dictate that the claims in the present invention are allowable.

Claim 23 recites one embodiment of a structure that has advantages over the bird's beak structure taught in the prior art. (*See* section VII.A.2, above). In this embodiment, the structure comprises a second isolated structure including a LOCOS isolation structure. The second isolated structure has an outer portion extending a first depth into the substrate and an inner portion including a second active region and extending a second depth into the substrate. The first depth is larger than the second depth.

As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests an isolated structure having an outer portion extending a first depth into a substrate and an inner portion containing an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. Moreover, the Applicant's statements describing the advantages of this structure over the prior art are never addressed, let alone challenged, in any

Office Action. As described below, for at least this additional reason, claim 23 is allowable over the teachings of Mehta, Yoo, and their combination.

Claims 24 and 25 are both dependent on the independent claim 23. As discussed above, the independent claim 23 is allowable over the teachings of Yoo, Mehta, and their combination. Accordingly, claims 24 and 25 are both also allowable as being dependent on an allowable base claim.

The independent claim 26 is directed to a system containing a semiconductor device having a plurality of isolated structures. The system of claim 26 comprises a common substrate having a first area including an STI isolation structure and a second area including a LOCOS isolation structure, the second area having an outer portion extending a first depth into the substrate and an inner portion including an active region extending a second depth into the substrate, wherein the first depth is larger than the second depth, an SRAM device implemented on the first area of the substrate and a flash EPROM device implemented on the second area of the substrate.

As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests an isolated structure having an outer portion extending a first depth into a substrate and an inner portion containing an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. The advantages of this structure are not addressed in any Office Action. For at least these reasons, claim 26 is allowable over the teachings of Mehta, Yoo, and their combination.

Claims 27 and 28 are both dependent on the independent claim 26. As discussed above, the independent claim 26 is allowable over the teachings of Yoo, Mehta, and their combination. Accordingly, claims 27 and 28 are both also allowable as being dependent on an allowable base claim.

7. In the "Response to Arguments" section, the final Office Action ignores the teachings of Mehta.

At page 4 of the final Office Action, it is stated (bolding added):

> Applicant further contends that Mehta does not teach STI trench. It should be noted that STI is a b[r]oad term that is used to describe a deep trench in a semiconductor substrate. It is recognizable to one of ordinary skill in the art regardless of how it is made. **A deep trench may be considered as an STI trench.** Mehta provides a way to modifies [sic] the process of making STI trench, for example, avoiding masking. However, Mehta realizes that an STI trench is capable of providing its function as isolation.

The Applicants respectfully disagree with this statement for several reasons. First, as stated at page 3, line 25, of the Specification, STI stands for shallow trench isolation. Contrary to the assertion in the final Office Action, a deep trench may not be considered as an STI trench. Mehta does not teach a modified STI trench at all. Indeed, as described above, Mehta teaches against using an STI trench. At column 4, lines 50-53, Mehta specifically states that "The present invention provides significant advantages over the standard LOCOS process, shallow trench isolation (STI), or the self-aligned LOCOS trench (SALOT) processes."

Within the final Office Action, at pages 3-4, it is further stated:

> [T]he fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See Ex parte Obiaya, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). In this case, Mehta indeed discusses the advantage of using a modified STI trench (deep trench over LOCOS where low MOS spacing is necessary, for example, the area of the substrate. STI type trench provides minimum horizontal space, but deeper than LOCOS.

The Applicant respectfully disagrees with these statements for several reasons. First, and most important, Mehta does not teach a modified STI trench. Mehta teaches away from using an STI trench. Second, the prior art does not teach the present invention. Advantages offered by the Applicant flow from the present invention, not from the prior art.

B. BECAUSE THE FINAL OFFICE ACTION DID NOT ADDRESS THE APPLICANT'S ARGUMENTS THAT ITS CLAIM LIMITATIONS ARE NOT FOUND IN THE PRIOR ART, THESE CLAIM LIMITATIONS MUST BE FOUND TO DISTINGUISH THE CLAIMS OVER THE CITED REFERENCES.

Under M.P.E.P. § 707.07(f), an examiner should consider **all** arguments an applicant raises in traversing a rejection. Under § 707.07(f), if an applicant asserts that his invention has advantages over the prior art but the examiner believes that those advantages are not sufficient to overcome a rejection, the examiner should state in the record the reasons for his position. "By doing so the applicant will know that the asserted advantages have actually been considered by the examiner and, if appeal is taken, the Board of Patent Appeals and Interferences will also be advised." *Id.*

As part of its accompanying text, § 707.07(f) cites *In re Herrmann*, 261 F.2d 598 (C.C.P.A. 1958), a case that is directly on point here. In *In re Herrmann*, the Court of Customs and Patent Appeals reversed a rejection of claims for which the applicant had stated advantages. The CCPA found that it was "constrained" to accept the advantages argued by the applicant since they were not challenged by either the examiner or the Board of Appeals. 261 F.2d at 600. The CCPA thus was obliged to allow the claims at issue.

As described below, the final Office Action does not challenge, let alone even address, the Applicant's arguments raised in the May 2004 Response. In the May 2004 Response, the Applicants explained that the structures recited in its claims have advantages over the cited prior art. Specifically, the final Office Action does not challenge the Applicant's assertions that its invention differs from and has advantages over the bird's beak structure disclosed in the prior art. For at least these reasons, the independent claim 23 and its dependent claims 24 and 25, and the independent claim 26 and its dependent claims 27 and 28 are all allowable. Nor does the final Office Action challenge the Applicant's assertions in the May 2004 Response that embodiments of its invention advantageously have a single device layer that has both an active region and an STI isolation structure. For at least these reasons, the independent claim 18 and its dependent claims 21 and 22 are also all allowable.

This conclusion is also supported by the rules governing the examination of patents. Under those rules, during an examination of a patent, the PTO bears the initial burden of proving that the claims of a patent application are unpatentable. If the PTO fails to meet that burden, the claims are allowable. *In re Glaug*, 283 F.3d 1335, 1338 (Fed. Cir. 2002).

Here, the PTO has not met that burden because, by not even discussing the structures that the Applicant relies on in distinguishing its invention from the prior art, the PTO cannot make out a prima facie case of unpatentabilty. Accordingly, for this additional reason, the following claims are all allowable: independent claim 18 and its dependent claims 21 and 22; independent claim 23 and its dependent claims 24 and 25; and independent claim 26 and its dependent claims 27 and 28.

C. CONCLUSION

For the above reasons, it is respectfully submitted that the claims 1, 4-6, 9, 10, 18, and 21-28 are allowable over the cited prior art references. Therefore, a favorable indication is respectfully requested.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: December 20, 2004

By: Jonathan O. Owens
Jonathan O. Owens
Reg. No.: 37,902
Attorneys for Applicants

VIII. CLAIMS APPENDIX

This appendix includes a list of the claims under appeal.

Claim 1: A semiconductor device comprising:

a common substrate;

an SRAM device implemented on the common substrate and isolated by an STI isolation structure; and

a flash EPROM device implemented on the common substrate and isolated by a LOCOS isolation structure,

wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently.

Claims 2-3 (canceled)

Claim 4: The semiconductor device according to claim 1 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

Claim 5: A system containing different types of isolation structures, the system comprising:

a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently;

an SRAM device on the first portion of the substrate; and

a flash EPROM device on the second portion of the substrate.

Claim 6: The system according to claim 5 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

Claims 7-8 (canceled)

Claim 9: A semiconductor device comprising:

a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

Claim 10: The semiconductor device according to claim 9 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

Claims 11-17 (canceled)

Claim 18: A semiconductor device, comprising:

a common substrate;

a first portion formed on the common substrate, the first portion comprising an SRAM device over a first single device layer, the first single device layer comprising a first active region and an STI isolation structure; and

a second portion formed on the common substrate, the second portion comprising a flash EPROM device over a second single device layer, the second single device layer comprising a second active region and a LOCOS isolation structure.

Claims 19-20 (canceled)

Claim 21: The semiconductor device of claim 18, wherein the first single device layer comprises an insulating oxide.

Claim 22: The semiconductor device of claim 18, wherein the second single device layer comprises an insulating oxide.

Claim 23: A semiconductor device comprising:

a common substrate;

an SRAM device implemented on the common substrate and formed over a first active region on a first isolated structure including an STI isolation structure; and

a flash EPROM device implemented on the common substrate and formed over a second active region on a second isolated structure including a LOCOS isolation structure, the second isolated structure having an outer portion extending a first depth into the substrate and an inner portion including the second active region and extending a second depth into the substrate, the first depth larger than the second depth.

Claim 24: The semiconductor device of claim 23, wherein the first isolated structure and the second isolated structure are contiguous.

Claim 25: The semiconductor device of claim 23, wherein the first isolated structure and the second isolated structure both comprise an oxide material.

Claim 26: A system containing a semiconductor device having a plurality of isolated structures, the system comprising:

a common substrate having a first area including an STI isolation structure and a second area including a LOCOS isolation structure, the second area having an outer portion extending a first depth into the substrate and an inner portion including an active region extending a second depth into the substrate, wherein the first depth is larger than the second depth;

an SRAM device implemented on the first area of the substrate; and

a flash EPROM device implemented on the second area of the substrate.

Claim 27: The system of claim 26, wherein the first area and the second area are contiguous.

Claim 28: The system of claim 27, wherein the first area and the second area both comprise an oxide material.

IX. EXHIBITS

The following documents, which are part of the record, are attached for convenience:

Exhibit A: U.S. Patent Serial No. 5,605,853 to Yoo *et al.*

Exhibit B: U.S. Patent Serial No. 5,679,599 to Mehta